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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

CONTINUATION SHEET

Continuation of 11. does NOT place the application in condition for allowance because:

As to claim 19, Applicant's Attorney argues that the combination of Brightman (US 7,100,020; hereinafter Brightman) in view of Rosenthal (US 5,740,406; hereinafter Rosenthal) does not describe:

> 19. A device comprising:
>
> first circuitry to generate a packet based on packet header data received from and generated by a micro-engine and packet payload data from a memory controller, wherein the packet payload data bypasses the micro-engine, the first circuitry comprising
>
> second circuitry to receive the packet payload data from the memory controller, and to store the packet payload data in first-in first-out (FIFO) circuitry; and
>
> third circuitry to track a start lane in the FIFO circuitry indicating a start of free space in the FIFO circuitry, and to determine a starting lane for the packet payload data such that alignment of the packet payload data matches the start lane in the FIFO circuitry."

First argument of Applicant's Attorney details (at page 5, 1st ¶) that the combination of Brightman and Rosenthal does not describe, *"first circuitry to generate a packet based on packet header data received from and generated by a micro-engine..." (Emphasis added)."* Further on, Applicant's Attorney has supported the above-mentioned arguments with three specific points, namely:

i) First, there is no "Tx fabric processor 1605" (see page 5, 1st ¶).

ii) Second, the Tx fabric processor 1621 does not "generate a packet based on packet header data received from and generated by a micro-engine and packet payload data from a memory controller…" (see page 5, 1st ¶).

iii) Third, there is no support that Brightman describes the use of a micro-engine much less one that generates packet header data or that "packet payload data bypasses the micro-engine." (see page 6, 1st ¶).

However, the Examiner respectfully disagrees with the Applicant's Attorney and further assert that the combination of Brightman in view of Rosenthal shows the above-mentioned claim limitation.

Claim 19 is rejected in the Office Action (07/07/2009) under Brightman in view of Rosenthal as partially shown below for convenience:

*"**As to claim 19**, Brightman shows a device (Figure 2, packet switch 201) comprising:*

first circuitry (Figure 16, Fabric Processor 303) to generate a packet (Figure 16-18, col. 34, lines 29-46; note Tx fabric processor 1605 (part of Fabric Processor 303), makes a fabric frame 1801 based on headers 1803, 1805 and payload 1807)

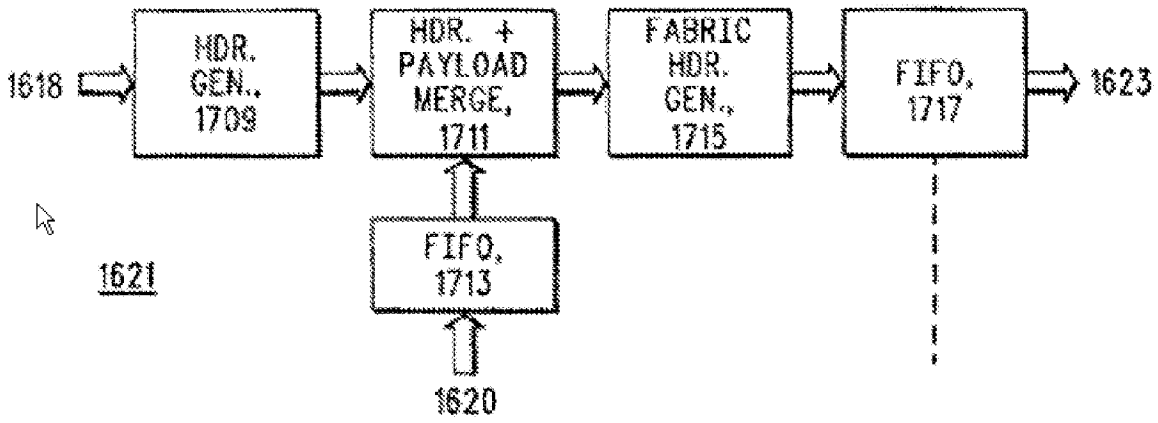
based on packet header data received from and generated by a micro-engine (Figure 16- 18; col. 35, lines 14-29; note that header 1805 is received from and generated by header generator 1709) and packet payload data from a memory controller (Figure 16-18; col. 35, lines 14-29; note payload 1807 is DMA'ed via path 1620 from buffer memory 229; col. 5, lines 13-22; note that DMA engine handles the DMA processes involving the transmit processor, buffer manager, and local memory.)

wherein the packet payload data bypasses the micro-engine (Figures 16-18; col. 35, lines 14-29; note that the header and the payload originate from different circuits and thus, the payload being DMA'ed from the buffer memory bypasses the header generators)…"

Regarding argument (i), Examiner agrees with the Applicant's Attorney that there is no "Tx fabric processor 1605". This is a minor error on the Examiner's part since the Examiner mainly wishes to point **"Tx fabric processor 1621"** instead of "Tx fabric processor 1605". There is only one "Tx fabric processor" in Figure 16 which is directed to part number 1621. Hopefully, this clarification will clear any misunderstanding between the rejection and the claimed invention. Examiner is grateful for the diligence and patience shown by the Applicant's Attorney.

Regarding argument (ii), Applicant's Attorney has specifically shown (see page 5-6) that "As discussed, no component of the Tx fabric processor 1621 "generate[s] a packet based on packet header data received from and generated by a micro- engine..." as the Tx fabric process generates, twice, a header information."

Brightman shows the following circuitry of the **Tx fabric processor 1621** in Figure 17:



Additionally, Brightman shows (col. 34, lines 29-46; col. 35, lines 14-28) the Tx fabric processor 1621 to include the first header generator (HDR. GEN. 1709) which generates a first header and second header generator (FABRIC HDR. GEN. 1715) which generates a second

header. By looking into 1709, 1719 and 1713, it can be seen that a packet header data (i.e. first header) is generated and received from the micro-engine (i.e. HDR. GEN. 1709) and is merged with a payload at circuitry HDR. + PAYLOAD MERGE 1711 to produce a frame (emphasis added). Brightman needs only to show one of the headers being merged with a payload to show the claimed generated packet. It is also noted that by merging the header with the payload (see Figure 17, 1711), the circuitry of Brightman shows a process of generating a packet as claimed.

It is also noted that the claim language presently claimed in claim 19, does not limit the claim to having **only** one means (i.e. circuitry) to generate a header. The system of Brightman shows two means of generating a header. However, the system of Brightman still applies to the claim language currently presented since Brightman shows not just one means (circuitry) to generate a header, but two means, which still applies to the currently presented claim language.

Thus, as seen above, even though Brightman shows a circuitry which produces two headers to merge with a payload, Brightman still shows a sub-circuit (part of) the main circuitry which produces a packet based from a header and a payload received from different components as claimed above.

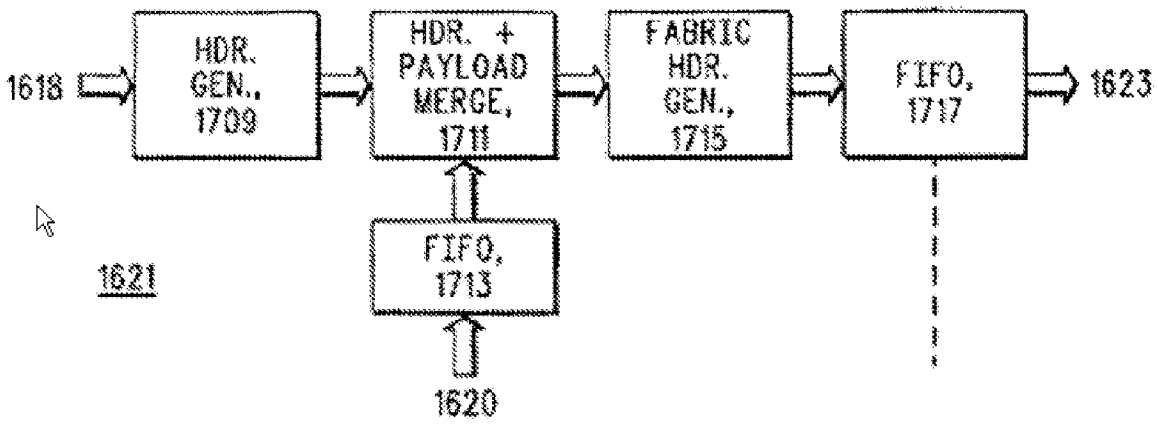
Regarding argument (iii), Applicant's Attorney additionally argues (see page 6, 1st ¶) that, "there is no support that Brightman describes the use of a micro-engine much less one that generates packet header data or that "packet payload data bypasses the micro-engine."

Examiner has already presented additional reasoning to apply to the argument "there is no support that Brightman describes the use of a micro-engine much less one that generates packet header data" as presented in the response to argument (ii) (see above section relating to

argument (ii).). Thus, the Examiner believes that the Applicant's Attorney wishes to argue mainly that Brightman does not show that the "packet payload data bypasses the micro-engine."

Examiner, again, will rely on Figure 17 of Brightman to show that Brightman indeed shows the claim limitation “"packet payload data bypasses the micro-engine."

Figure 17 of Brightman shows:



It can be seen that the header is generated and received from HDR 1709 and payload is received from FIFO 1713 (along with DMA engine – not shown) and is merged in HDR. + PAYLOAD MERGE 1711 to produce a first frame. It can be seen that the header (coming from the HDR GEN 1709) comes from a first path and payload (coming from FIFO 1713) comes from a different path from the first path.

Thus, one can see that the circuitry of Brightman shows at least the payload bypassing the micro-engine (HDR GEN 1709) as claimed.

Given the above-shown rejection and the additional reasoning presented with regards to arguments (i), (ii) and (iii), Brightman in view of Rosenthal shows the above-mentioned claim limitations.

Second argument of Applicant's Attorney details (at page 6, 2nd ¶) that the combination of Brightman and Rosenthal does not describe, the details of a third circuitry to track a start lane in the FIFO circuitry indicating a start of free space in the FIFO circuitry…"

Further on, Applicant's Attorney has supported the above-mentioned arguments with three specific points, namely:

i) First, the FIFO of Rosenthal stores commands not packet payload data.

ii) Second, Rosenthal, like Brightman, fails to show the details of circuitry to implement the operation of the pointers.

iii) Third, the combination does not describe circuitry "to determine a starting lane for the packet payload data such that alignment of the packet payload data matches the start lane in the FIFO circuitry."

iv) Finally, Applicants respectfully submit that one of ordinary skill in the art would not have reason nor be motivated to combine the cited references in the manner purported by the Office Action and moreover, there has been no showing that there would be motivation to add the pointer functionality to Brightman's FIFO which apparently works just fine without it.

However, the Examiner respectfully disagrees with the Applicant's Attorney and further assert that the combination of Brightman in view of Rosenthal shows the above-mentioned claim limitation.

Claim 19 is rejected in the Office Action (07/07/2009) under Brightman in view of Rosenthal as partially shown below for convenience:

"Even though, Brightman shows the use of a FIFO buffer in receiving payload in order to deal with delays, as discussed above, Brightman does not specifically show the details of a third circuitry to track a start lane in the FIFO circuitry indicating a start of free space in the FIFO circuitry, and to determine a starting lane for the .packet payload data such that alignment of the ~payload data matches the start lane in the FIFO circuitry.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Rosenthal. Specifically, Rosenthal shows a third circuitry to track a start lane in the FIFO circuitry indicating a start of free space in the FIFO circuitry, and to determine a starting lane for the .packet payload data (Figure 7; col. 16, line 34 to col. 17, line 42; note pointers are utilized to define the positions of the beginning and end of the individual FIFO buffers 39 and the beginning and end of the data; further note that a FIFO buffer 39 which is initially empty and provides a maximum free count value when read by the central processing unit will provide a lower free count number after the amount of data first indicated by the free count register has been sent.) such that alignment of the packet payload data matches the start lane in the FIFO circuitry (Figure 7; col. 16, line 34 to col. 17, line 42; note the use of such pointers allows alignment of data with corresponding FIFO positions).

In view of the above, having the system of Brightman, then given the well-established teaching of Rosenthal, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Brightman as taught by Rosenthal, in order to allow an application know that sufficient space will be available for a given operation (col. 17, lines 15- 16)."

Regarding argument (i), Applicant's Attorney argues that Rosenthal stores commands and not packet payload data.

It should be noted that the Examiner has already shown the claim limitation "packet payload data" using Brightman (Figure 17; col. 34, line 29-46; col. 35, line 14-28) where packet payload data is forwarded from FIFO 1713 (along with DMA engine – not shown). Brightman

does not specifically show the structure and the functionalities of FIFO 1713 and thus, Rosenthal was introduced in order to show the specific structure and functionalities of a FIFO as claimed in claim 19. Thus, the Examiner has used Rosenthal to show how data (i.e. command) is stored in the FIFO as claimed.

Regarding argument (ii), Applicant's Attorney argues generally, that Brightman in view of Rosenthal fails to show the details of the circuitry to implement the operation of the pointers.

However, it should be noted that, as seen in the above rejection, the Examiner has shown specific parts of Rosenthal, namely, Figure 7; col. 16, line 34 to col. 17, line 42 (see Office Action dated 07/07/2009, page 4, 3rd ¶ for details) to show the details of the circuitry to implement the operation of the pointers as argued by the Applicant's Attorney.

Regarding argument (iii), Applicant's Attorney argues that the combination does not describe circuitry "to determine a starting lane for the packet payload data such that alignment of the packet payload data matches the start lane in the FIFO circuitry" and specifically mentions that [the pointers] does not assist in alignment of anything.

The claimed invention presented in claim 19 requires at least the function "to determine a starting lane for the packet payload data such that alignment of the packet payload data matches the start lane in the FIFO circuitry." Examiner has rejected the above claim limitations using Rosenthal's Figure 7, col. 16, line 34 to col. 17, line 42. Specifically, the pointers (see col. 16, line 63-65) of Rosenthal are utilized to define the positions (i.e. starting lane) of the beginning and end of the individual FIFO buffers and the beginning and end of the data. The value of the pointer is held by a flow control register. Thus, initially given a data placed in an empty FIFO,

the value of the pointer in the flow control register points out the alignment of the (beginning) of the data to the beginning of the FIFO.

Thus, in this instance, the pointers of Rosenthal also assists in the alignment of at least something, and is also in-line with the claim limitations presented in claim 19.

Regarding argument (iv), Applicant's Attorney that "one of ordinary skill in the art would not have reason nor be motivated to combine the cited references in the manner purported by the Office Action and moreover, there has been no showing that there would be motivation to add the pointer functionality to Brightman's FIFO which apparently works just fine without it."

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In this case, the system of Brightman deals with an integrated circuit for use in processing streams of packets for transmission and reception (see abstract) wherein the system also shows a DMA engine which provides DMA access between transmit processor and the buffer manager as well as the local memory and the buffer manager (see col. 5, lines 13-18; col. 34, line 29-46; col. 35, line 14-28). However, the system of Brightman lacks the specific details of the FIFO management/functionalities as claimed. Thus, the Examiner has introduced Rosenthal, in order to specifically show the FIFO management/functionalities. Similar to Brightman, Rosenthal uses

a DMA engine (see Figure 3; col. 4, line 14-29) which also provides DMA operations pertaining to memory (i.e. FIFO) management.

Thus, one of ordinary skill in the art would have been motivated to combine Brightman and Rosenthal, and such combination will allow an application know that sufficient space will be available for a given operation (as stated in rejection of claim 19).

Given the above-shown rejection and the additional reasoning presented with regards to arguments (i)-(iv), Brightman in view of Rosenthal shows the above-mentioned claim limitations.

As to claims 20-23, Applicant's Attorney has presented arguments based on the same argument presented in claims 19. The Examiner has addressed the argument presented in claim 19 and thus applies the same reasoning to claims 20-23.

/Redentor M Pasia/
Examiner, Art Unit 2416

/Aung S. Moe/

Supervisory Patent Examiner, Art Unit 2416